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(71) Applicant: Kabushiki Kaisha Toshiba
72, Horikawa-cho Saiwai-ku
Kawasaki-shi Kanagawa-ken 210(JP)

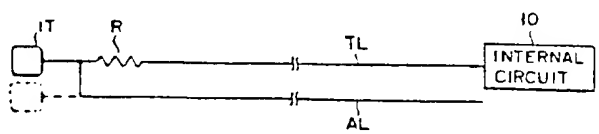
(72) Inventor: Yasuda, Hiroshi c/o Patent Division
Kabushiki Kaisha Toshiba 1-1 Shibaura 1-chome
Minato-ku Tokyo 105(JP)

(74) Representative: Eitle, Werner, Dipl.-Ing. et al,
Hoffmann, Eitle & Partner Patentanwälte Arabellastrasse 4
D-8000 München 81(DE)

(54) Signal transmission circuit in a semiconductor integrated circuit.

(57) A signal transmission circuit includes an input pad (IT) for receiving an input signal, a resistor (R) connected at one end to the input pad, and a signal transmission line (TL) connected at the input end to the other end of the resistor (R), and at the output end to an internal circuit (10). The signal transmission circuit further includes an auxiliary line (AL) connected at the input end to the input pad (IT), floating electrically at the output end, and extending substantially in parallel with the transmission line (TL).

F I G. 9



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Signal transmission circuit in a semiconductor integrated circuit

The present invention relates to a signal transmission circuit used in a semiconductor integrated circuit.

In integrated circuits, it is often required to deliver a signal over substantially the total area of the semiconductor chip, or to transmit a signal from a first point on the chip to a second point far distanced from the first point. This being the case, a relatively long transmission line is used. This long transmission line is usually a metal resistivity having the smallest possible resistance such as aluminum. A large stray capacitance exists between the metal transmission line and the silicon substrate or other such conductive layer. The longer the transmission line, the larger the stray capacitance. This stray capacitance delays propagation of a signal through the transmission line, and hence adversely influences the operating characteristics of the integrated circuit.

As shown in Fig. 1, an input signal is supplied to an input pad 1 formed on an IC chip 2. The signal is further transmitted to an internal circuit 5 through a protective resistor 3 and a long interconnection line or a signal transmission line 4. The protective resistor 3 protects the internal circuit 5 from an abnormally high voltage accidentally applied to the

input pad 1. For this reason, the protective resistor 3 has a high resistance, usually 1 to 2 kilo ohms. The resistor 3 cooperates with the stray capacitance associated with the transmission line 4, to greatly delay propagation of the signal through the transmission line 4.

The stray capacitance associated with the transmission line 4 is the sum of the capacitance C1 between the transmission line 4 and the semiconductor substrate 6, and the capacitance C2 between the transmission line 4 and its adjacent interconnection lines 7. In an integrated circuit of a high circuit density, the distance between the lines 4 and 7 is short. The stray capacitance associated with the transmission line 4, therefore, is effectively influenced by the stray capacitance C2. Thus, as the interconnection lines are laid closer to each other, the stray capacitance associated with the transmission line 4 becomes larger, lowering the signal propagating speed.

Accordingly, an object of the present invention is to provide a signal transmission circuit which effectively reduces a stray capacitance associated with a signal transmission line during signal transmission, thereby achieving high-speed signal transmission.

To achieve the above object, there is provided a signal transmission circuit comprising a signal transmission line formed on a semiconductor integrated circuit chip, an auxiliary line capacitively coupled with the transmission line, and a signal supplying circuit for supplying the first input signal to the transmission line, and for supplying, to the input end of the auxiliary line, a second input signal changing in the same direction as the first input signal, but at a greater rate of change.

Because the second input signal changes in the same direction on the first input signal, but at a greater

rate of change, the effective value of capacitance between the transmission and the auxiliary lines becomes negative, to thereby reduce the stray capacitance associated with the transmission line. Therefore, transmission speed of the first signal on the transmission line is improved.

This invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

Fig. 1 schematically illustrates a signal transmission circuit of the prior art;

Fig. 2 illustrates stray capacitances among a transmission line, a substrate and adjacent interconnection lines in the circuit of Fig. 1;

Fig. 3 shows a graph illustrating an effective value of a stray capacitance, between two transmission lines, against the ratio of change rates of signals which propagate through these transmission lines;

Fig. 4 is a circuit diagram of a signal transmission circuit according to an embodiment of the present invention;

Figs. 5 and 6 are circuit diagrams of two examples of the wave shaping circuit used in Fig. 4;

Fig. 7 illustrates stray capacitances existing between the transmission line, the auxiliary line and the substrate of the Figs. 5 and 6 circuits;

Fig. 8 shows operating characteristics of the signal transmission circuits shown in Figs. 1 and 4;

Fig. 9 is a circuit diagram of a signal transmission circuit according to another embodiment of the present invention; and

Fig. 10 shows stray capacitances existing between the transmission line, the substrate and auxiliary lines of Fig. 9 when the auxiliary lines are disposed on both sides of and above the transmission line.

The inventor of the present invention has studied how an effective value of a stray capacitance

associated with the signal transmission line on an IC chip varies while the IC circuit is operating. As already described referring to Fig. 2, because the substrate potential is fixed, the stray capacitance C1 existing between the transmission line 4 and the substrate 6 has a constant value. The effective value of the capacitance C2 existing between the interconnection lines 4 and 7 varies depending upon the potential difference ΔV between these interconnection lines 4 and 7 and the signal current i flowing through the transmission line 4. It is assumed that, when the interconnection line 7 is held at a given voltage, the effective value of the stray capacitance C2 will have a fixed value CO. On this assumption, if the potentials between the interconnection lines 4 and 7 vary at an equal rate of change in opposite directions, the effective value of the capacitance C2 will be 2CO. If these potentials vary at an equal rate of change in the same direction, the effective value of the capacitor C2 will be 0. When the potentials on the lines 7 and 4 vary in the same direction, but the rate of change of the former is two times that of the latter, the stray capacitance C2 is - CO, and the effective value of the total of the stray capacitances associated with the transmission line 4 becomes small. Therefore, a signal can be propagated on the transmission line 4 at a higher speed.

Fig. 3 shows the relationship between an effective value of the stray capacitance C2 and the variation rate of the potential on the line 7 when the potential on the line 4 is changed at a predetermined rate of variation V1. As seen, to reduce the effective value of the stray capacitance associated with the transmission line 4, it is necessary to vary the potential on the line 7 in the same direction as the potential on the line 4, but at a larger rate of change.

The conclusion deducted from the above fact is

that the signal propagating speed on the transmission line 4 can be increased by appropriately changing the potential on the interconnection line or the adjacent line 7 in connection with a potential variation on the line 4.

Fig. 4 shows a signal transmission circuit according to an embodiment of the present invention. The signal transmission circuit includes a transmission line TL and an auxiliary line AL. A signal, which is supplied to an input terminal IT and passed through a protective resistor R, is transmitted to an internal circuit 10 by this signal transmission circuit. The auxiliary line AL is laid substantially in parallel with the transmission line TL. The input end of the auxiliary line AL is connected to the output terminal of a wave shaping circuit 12. This wave shaping circuit 12, which includes inverters 12A and 12B, shapes a waveform of the signal from the protective resistor R. The output end of the auxiliary line AL floats electrically.

Two examples of the wave shaping circuit 12 are shown in Figs. 5 and 6. The Fig. 5 circuit is a CMOS device including p-channel MOS transistors 12A1 and 12B1, and n-channel MOS transistors 12A2 and 12B2. The Fig. 6 circuit is an NMOS device including n-channel enhancement type MOS transistors 12A3 and 12B3, and n-channel depletion type MOS transistors 12A4 and 12B4.

Fig. 7 illustrates stray capacitances existing in these signal transmission circuits. CX denotes a stray capacitance existing between the transmission line TL and the auxiliary line AL. CY represents a stray capacitance existing between the transmission line TL and the semiconductor substrate 14. The transmission line TL is further coupled, at its output end, with a load capacitance of the internal circuit 10. In total, therefore, a large capacitor is coupled with the

transmission line TL. Thus, the signal propagates through a signal transmission circuit that includes a large resistance protective resistor R and a large capacitance transmission line TL. This largely delays the signal transmission. Thus, when an input signal is rapidly changed the potential on the transmission line TL changes at a rate relatively smaller than the rate of the signal change. On the other hand, the auxiliary line AL is in a floating state at the far or output end. Therefore, the stray capacitance associated with the auxiliary line AL is considerably smaller than that associated with thetransmission line TL.

The same signal as applied to the transmission line TL is applied to the input end of the auxiliary line AL after it is waveshaped by the wave shaping circuit 12. For this reason, the signal supplied to the auxiliary line AL changes at a greater rate of change, and in the same direction, than the signal supplied to the transmission line TL. The stray capacitance associated with the auxiliary line AL is markedly smaller than that associated with the transmission line TL. The signal delay caused in the auxiliary line AL is smaller than that in the transmission line TL.

Fig. 8 illustrates how the potentials at the output ends of the lines AL and TL vary when a signal with a specific rise curve is supplied to the input terminal IT. In this case, the input signal is changed from "0" level to a predetermined level at time t0, and kept at the predetermined level. The output ends of the lines TL and AL are substantially equally distanced from the input terminal IT.

In Fig. 8, curve A, as depicted by a continuous line, represents a variation of the potential PT on the transmission line TL. Curve B, shown by a one-dot chain line, represents a variation of the potential PA on the auxiliary line AL. Curve C indicates a variation of the potential PL on the transmission line TL when the

auxiliary line AL is not used.

As shown, the potential PA on the auxiliary line AL rises after a predetermined time from the rise of the potential PT on the transmission line TL. This is because the signal is delayed by the wave shaping circuit 12. The potential PA rises at a relatively great rate, such that it then exceeds the potential PT. At this time, the effective value of the stray capacitance C2 existing between the lines TL and AL becomes small, as described in Fig. 3. Accordingly, the potential PT on the line TL rises at a larger variation rate toward the VH level, as shown by the curve A.

By setting the interval between the lines TL and AL to the minimum value tolerated in design, the between-line capacitance can be enlarged. In this case, due to a potential variation on the auxiliary line AL, it is possible to greatly reduce the effective value of the stray capacitance associated with the transmission line TL.

Fig. 9, shows a signal transmission circuit according to another embodiment of the present invention. This embodiment is different from the Fig. 4 embodiment in the following respect. In this embodiment, the wave shaping circuit 12 is omitted by connecting the input end of the auxiliary line AL directly to the junction between the input terminal IT and the protective resistor R. A signal supplied to the input terminal IT is transmitted through the resistor R to the transmission line TL, and, at the same time, directly to the auxiliary line AL. Note here that if a high voltage signal is applied to the input terminal IT and directly to the auxiliary line AL, it will not, under any circumstances, destroy the integrated circuit. The reason for this is that the output end of the auxiliary line AL is in an open state.

Because of the direct connection of the line AL to the terminal IT, the potential on the line AL quickly

changes according to the input signal at the terminal IT. Further, since the wave shaping circuit 12 is not used in this circuit, the potential on the auxiliary line AL immediately changes in accordance with a change of the input signal. For example, when the input signal rapidly and sharply rises to the level VH, as in Fig. 8, the potential on the auxiliary line AL starts to rise at an earlier timing than in the case of Fig. 8.

The signal is applied through the protective resistor R to the transmission line TL. Therefore, the signal on the transmission line TL changes in accordance with a change in the input signal with a time delay. Accordingly, the potential PA on the auxiliary line AL starts to change at the same timing and in the same direction as the potential PT on the transmission line TL, and then changes at a greater rate of variation than the potential PT. Therefore, the effective value of the stray capacitance associated with the transmission line TL is reduced, so that the signal is quickly propagated to the internal circuit 10.

It should be understood that the present invention is not limited to the two specific embodiments explained above. For example, in the above-mentioned embodiments, the auxiliary line AL is disposed in parallel on only one side of the transmission line TL. It may, however, be disposed on both sides of and/or above the transmission line TL. The example shown in Fig. 10 has the auxiliary lines AL on both sides of and above the transmission line TL. By laying an auxiliary line UAL above the transmission line TL with a thin insulating layer disposed therebetween, the capacitance between the lines TL and the line UAL can readily be increased. Therefore, the effective value of the capacitance can be reduced to considerably improve the signal transmission characteristic of the signal transmission circuit.

In a modification of the embodiment of Fig. 9, the

input end of the auxiliary line AL is disconnected from the input terminal IT and connected to an additional input pad, as indicated by a broken line in Fig. 9. This modification, by supplying the same input signal as supplied to the input terminal IT to the additional pad, has the same useful effect as the Fig. 9 embodiment.

Claims:

1. A signal transmission circuit including a signal transmission line (TL) formed on a semiconductor integrated circuit chip, and signal supplying means (IT, R) for supplying a first input signal to the input end of said transmission line (TL); characterized in that an auxiliary line (AL) is provided capacitively coupled with said transmission line (TL), and said signal supplying means (IT, R, 12) supplies, to the input end of said auxiliary line (AL), a second input signal which changes in the same direction as the first input signal, but at a larger rate of change than the first input signal.

2. A signal transmission circuit according to claim 1, characterized in that said signal supplying means includes a signal input pad (IT) for receiving an input signal, and resistor means (R) coupled between said signal input pad (IT) and said transmission line (TL).

3. A signal transmission circuit according to claim 2, characterized in that said signal supplying means further includes waveshaping means (12) connected at the input terminal to the junction between the input end of said transmission line (TL) and said resistor means (R), and at the output terminal to the input end of said auxiliary line (AL).

4. A signal transmission circuit according to claim 3, characterized in that said auxiliary line (AL) includes one of the conductive lines formed on both sides of and above said transmission line (TL), each of said conductive lines being connected at the input end to the output terminal of said waveshaping means (12), floating electrically at the output end, and extending substantially in parallel with said transmission line (TL).

5. A signal transmission circuit according to

claim 2, characterized in that said auxiliary line (AL) includes at least one of the conductive lines formed on both sides of and above said transmission line (TL), each of said conductive lines being connected at the input end to the junction between said signal input pad (IT) and said resistor means (R), floating electrically at the output end, and extending substantially in parallel with said transmission line (TL).

6. A signal transmission circuit according to claim 2, characterized in that said signal supplying means has an additional input pad connected to the input end of said auxiliary line (AL), said additional input pad receiving the same input signal as that supplied to said signal input pad (IT).

7. A signal transmission circuit according to claim 6, characterized in that said auxiliary line (AL) includes at least one of the conductive lines formed on both sides of and above said transmission line (TL), each of said conductive lines being connected at the input end to said additional input pad, floating electrically at the output end, and extending substantially in parallel with said transmission line (TL).

FIG. 1

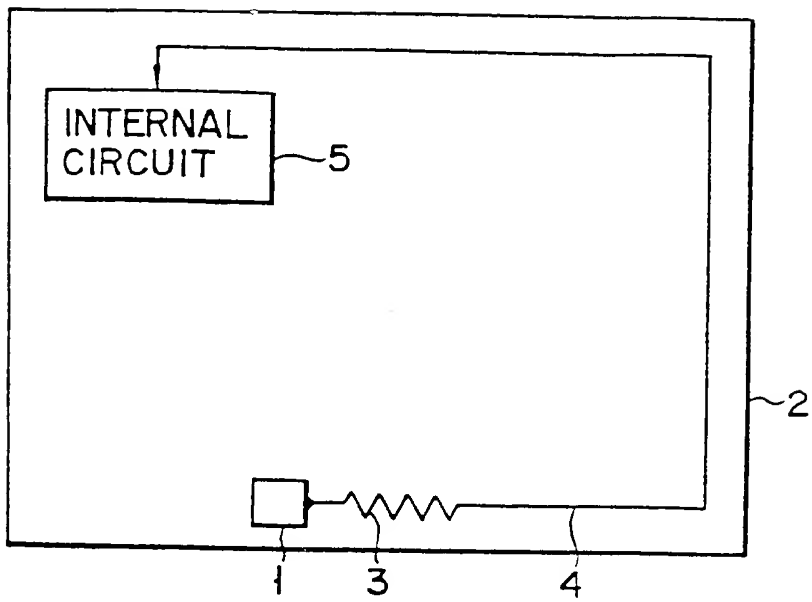


FIG. 2

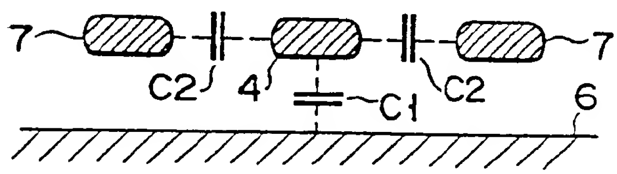
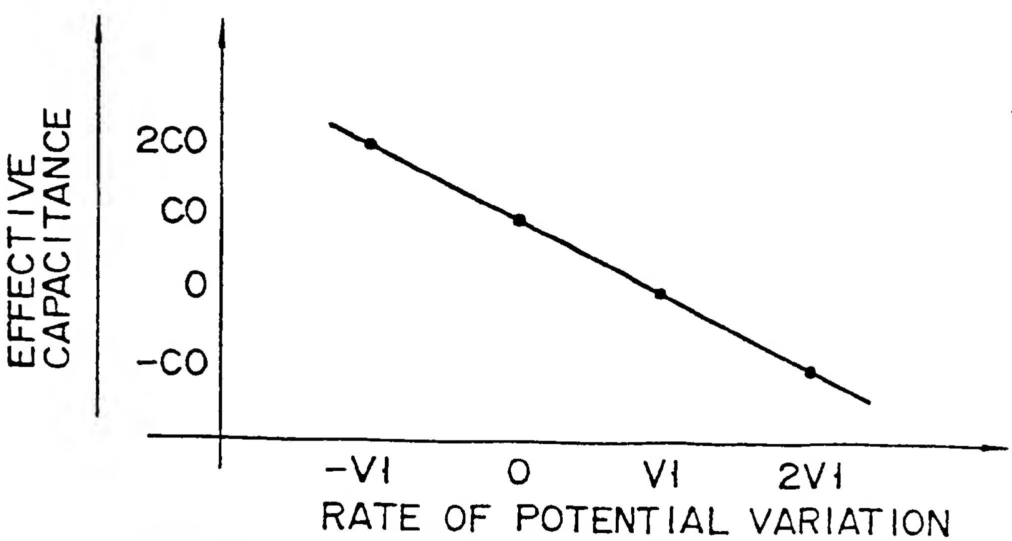
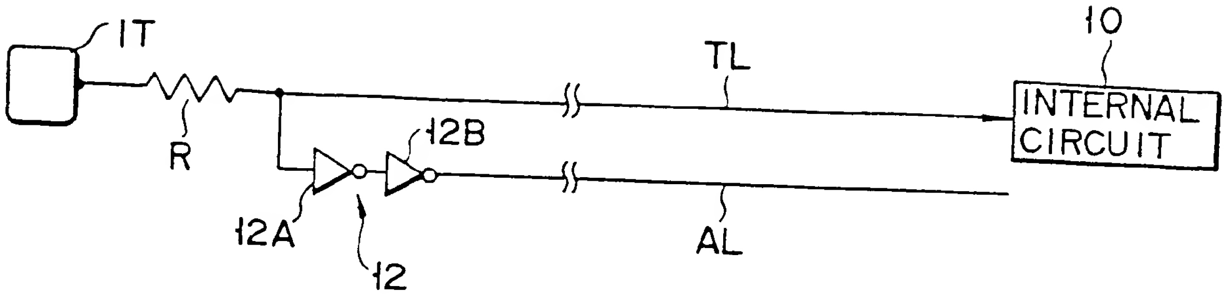


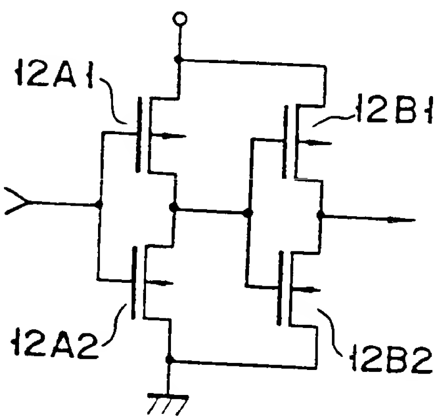
FIG. 3



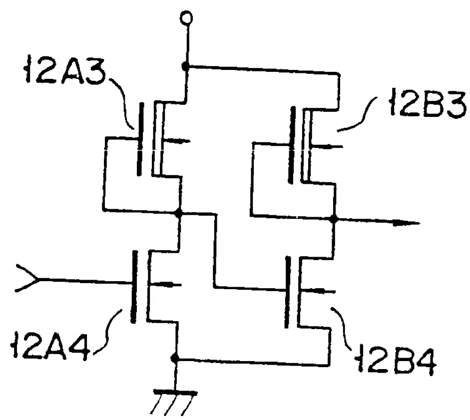
F I G. 4



F I G. 5



F I G. 6



F I G. 7

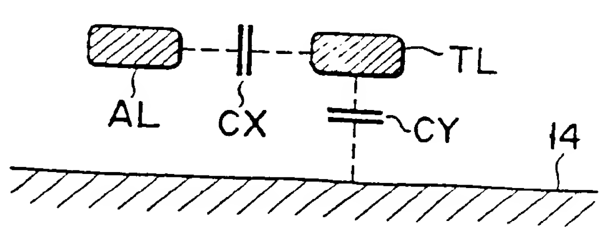


FIG. 8

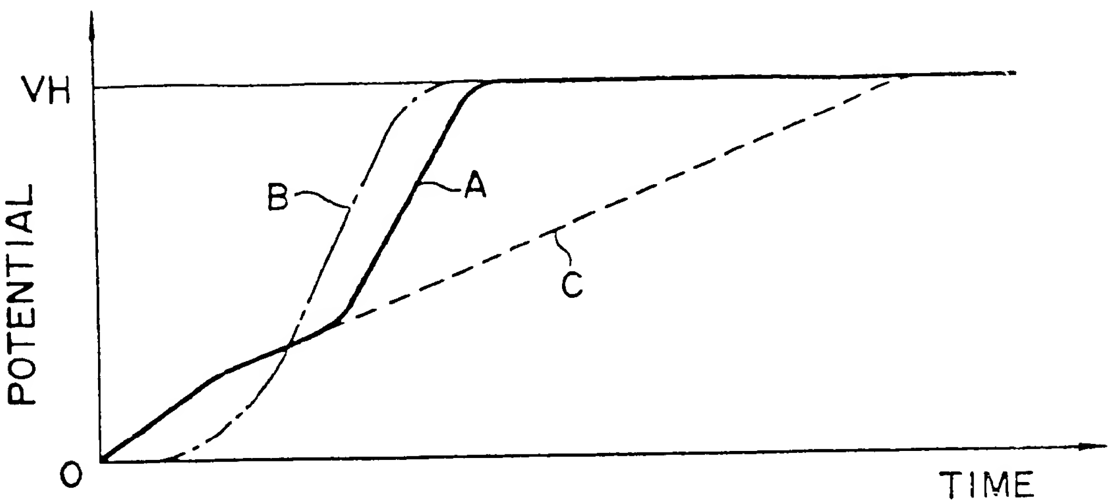


FIG. 9

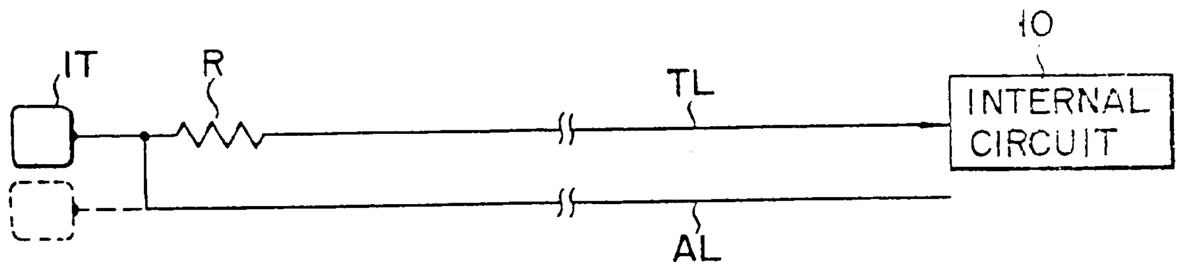


FIG. 10